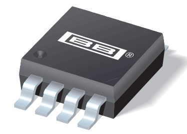


SBAS226 – MARCH 2002

16-Bit, High-Speed, 2.7V to 5.5V *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **16-BITS NO MISSING CODES**
- **VERY LOW NOISE: 3LSBp-p**
- **EXCELLENT LINEARITY: ±1.5LSB typ**
- ***micro*POWER: 4.5mW at 100kHz**
  1mW at 10kHz
- **MSOP-8 PACKAGE**
- **16-BIT UPGRADE TO THE 12-BIT ADS7816 AND ADS7822**
- **PIN-COMPATIBLE WITH THE ADS7816, ADS7822, AND ADS8320**
- **SERIAL (SPI™/SSI) INTERFACE**

APPLICATIONS

- **BATTERY-OPERATED SYSTEMS**
- **REMOTE DATA ACQUISITION**
- **ISOLATED DATA ACQUISITION**
- **SIMULTANEOUS SAMPLING, MULTI-CHANNEL SYSTEMS**
- **INDUSTRIAL CONTROLS**
- **ROBOTICS**
- **VIBRATION ANALYSIS**

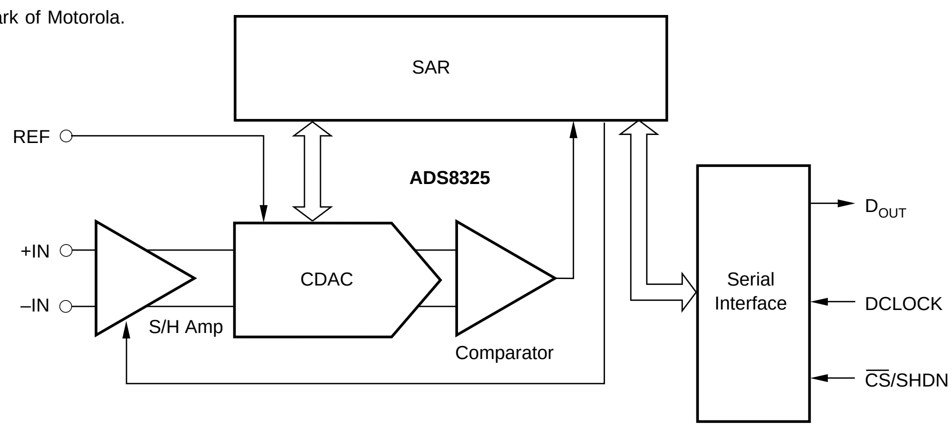
SPI is a registered trademark of Motorola.

DESCRIPTION

The ADS8325 is a 16-bit, sampling, Analog-to-Digital (A/D) converter specified for a supply voltage range from 2.7V to 5.5V. It requires very little power, even when operating at the full 100kHz data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode. For example, the average power dissipation is less than 1mW at a 10kHz data rate.

The ADS8325 offers excellent linearity and very low noise and distortion. It also features a synchronous serial (SPI/SSI compatible) interface and a differential input. The reference voltage can be set to any level within the range of 2.5V to V_{DD}.

Low power and small size make the ADS8325 ideal for portable and battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS8325 is available in an MSOP-8 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Absolute Maximum Ratings over operating free-air temperature, unless otherwise noted.

Supply Voltage, DGND to V_{DD}	–0.3V to 6V
Analog Input Voltage[2]	–0.3V to V_{DD} + 0.3V
Reference Input Voltage[2]	–0.3V to V_{DD} + 0.3V
Digital Input Voltage[2]	–0.3V to V_{DD} + 0.3V
Input Current to Any Pin Except Supply	–20mA to 20mA
Power Dissipation	See Dissipation Rating Table
Operating Virtual Junction Temperature Range, T_J	–40°C to +150°C
Operating Free-Air Temperature Range, T_A	–40°C to +85°C
Storage Temperature Range, T_{STG}	–65°C to +150°C
Lead Temperature 1.6mm (1/16 inch) from Case for 10sec	260°C

NOTES: (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions of extended periods may affect device reliability. (2) All voltage values are with respect to ground terminal.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

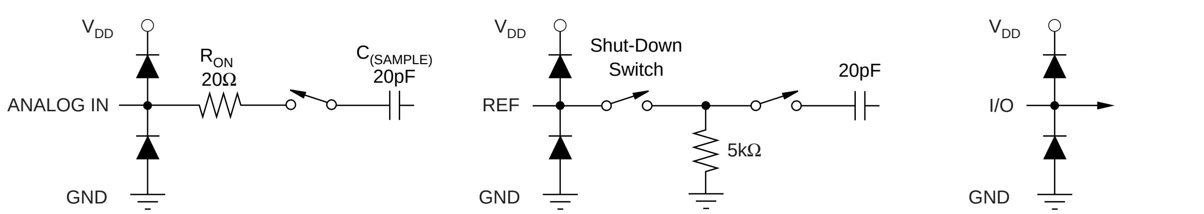
PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)[1]	PACKAGE-LEAD	PACKAGE DESIGNATOR[2]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8325I	±6	15	MSOP-8	DGK	–40°C to 85°C	B25	ADS8325IDGKT	Tape and Reel, 250
"	"	"	"	"	"	"	ADS8325IDGKR	Tape and Reel, 2500
ADS8325IB	±4	16	MSOP-8	DGK	–40°C to 85°C	B25	ADS8325IBDGKT	Tape and Reel, 250
"	"	"	"	"	"	"	ADS8325IBDGKR	Tape and Reel, 2500

NOTE: (1) No Missing Codes Error specifies a 5V power supply and reference voltage. (2) For the most current specifications and package information, refer to our web site at www.ti.com.

PACKAGE DISSIPATION RATING TABLE

PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGK	39.1°C/W	206.3°C/W	4.847mW/°C	606mW	388mW	315mW

EQUIVALENT INPUT CIRCUIT



Diode Turn-On Voltage: 0.35V

Equivalent Analog Input Circuit

Equivalent Reference Input Circuit

Equivalent Digital Input/Output Circuit

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply Voltage GND to V_{DD}	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5	5.0	5.5	V
Reference Input Voltage		2.5		V_{DD}	V
Analog Input Voltage	–IN	–0.3	0	0.5	V
	+IN – (–IN)	0		V_{REF}	V
Operating Junction Temperature Range, T_J		–40		125	°C

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = +5V, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE}, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8325I			ADS8325IB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
Full-Scale Range	FSR	+IN – (–IN)	0		V_{REF}	∗		∗	V
Operating Common-Mode Signal			–0.3		0.5	∗		∗	V
Input Resistance		–IN = GND		5			∗		GΩ
Input Capacitance		–IN = GND, During Sampling		45			∗		pF
Input Leakage Current		–IN = GND		±50			∗		nA
Differential Input Capacitance		+IN to –IN, During Sampling		20			∗		pF
Full-Power Bandwith	FSBW	f_S Sinewave, SINAD at –3dB		20			∗		kHz
DC ACCURACY									
Resolution			16			∗			Bits
No Missing Code	NMC		15			16			Bits
Integral Linearity Error	INL			±3	±6		±1.5	±4	LSB
Offset Error	V_{OS}			±0.75	±1.5		±0.5	±1	mV
Offset Error Drift	TCV_{OS}			±0.2			∗		ppm/°C
Gain Error	G_{ERR}				±24			±12	LSB
Gain Error Drift	TCG_{ERR}			±0.3			∗		ppm/°C
Noise				20			∗		µVRMS
Power-Supply Rejection		4.75V ≤ V_{DD} ≤ 5.25		3			∗		LSB
SAMPLING DYNAMICS									
Conversion Time	t_{CONV}	24kHz < f_{CLK} ≤ 2.4MHz	6.667		666.7	∗		∗	µs
Acquisition Time	t_{AQ}	f_{CLK} = 2.4MHz	1.875			∗			µs
Throughout Rate					100			∗	kSPS
Clock Frequency			0.024		2.4	∗		∗	MHz
AC ACCURACY									
Total Harmonic Distortion	THD	5Vp-p Sinewave, at 1kHz		–100			–106		dB
Spurious-Free Dynamic Range	SFDR	5Vp-p Sinewave, at 1kHz		–100			–108		dB
Signal-to-Noise Ratio	SNR			–90			–91		dB
Signal-to-Noise + Distortion	SINAD	5Vp-p Sinewave, at 1kHz		–90			–91		dB
Effective Number of Bits	ENOB			14.6			14.7		Bits
VOLTAGE REFERENCE INPUT									
Reference Voltage			2.5		V_{DD} + 0.3	∗		∗	V
Reference Input Resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			∗		kΩ
		$\overline{CS}$ = V_{DD}		5			∗		GΩ
Reference Input Capacitance				20			∗		pF
Reference Input Current				1	1.5		∗	∗	mA
		$\overline{CS}$ = V_{DD}		0.1			∗	∗	µA
DIGITAL INPUTS(1)									
Logic Family				CMOS			∗		
High-Level Input Voltage	V_{IH}		0.7 • V_{DD}		V_{DD} + 0.3	∗		∗	V
Low-Level Input Voltage	V_{IL}		–0.3		0.3 • V_{DD}	∗		∗	V
Input Current	I_{IN}	V_I = V_{DD} or GND			±50				nA
Input Capacitance	C_I			5			∗		pF
DIGITAL OUTPUTS(1)									
Logic Family				CMOS			∗		
High-Level Output Voltage	V_{OH}	V_{DD} = 4.5V, I_{OH} = –100µA	4.44			∗			V
Low-Level Output Voltage	V_{OL}	V_{DD} = 4.5V, I_{OL} = 100µA			0.5			∗	V
High-Impedance-State Output Current	I_{OZ}	$\overline{CS}$ = V_{DD}, V_I = V_{DD} or GND			±50			∗	nA
Output Capacitance	C_O			5			∗		pF
Load Capacitance	C_L				30			∗	pF
Data Format				Straight Binary			∗		

∗ indicates the same specifications as the ADS8325I.

NOTE: (1) Applies for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.

ELECTRICAL CHARACTERISTICS: V_{DD} = +2.7V

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = +2.5V, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE}, unless otherwise noted.

			ADS8325I			ADS8325IB			
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG INPUT									
Full-Scale Range	FSR	+IN – (–IN)	0		V_{REF}	*		*	V
Operating Common-Mode Signal			–0.3		0.5	*		*	V
Input Resistance		–IN = GND		5			*		GΩ
Input Capacitance		–IN = GND, During Sampling		45			*		pF
Input Leakage Current		–IN = GND		±50			*		nA
Differential Input Capacitance		+IN to –IN, During Sampling		20			*		pF
Full-Power Bandwith	FSBW	f_S Sinewave, SINAD at –3dB		4			*		kHz
DC ACCURACY									
Resolution		16			*			Bits	
No Missing Code	NMC		14			15			Bits
Integral Linearity Error	INL			±3	±6		±1.5	±4	LSB
Offset Error	V_{OS}			±0.75	±1.5		±0.5	±1	mV
Offset Error Drift	TCV_{OS}			±3			*		ppm/°C
Gain Error	G_{ERR}			±33			±16		LSB
Gain Error Drift	TCG_{ERR}			±0.3			*		ppm/°C
Noise				20			*		µVRMS
Power-Supply Rejection		2.7V ≤ V_{DD} ≤ 3.6V		7			*		LSB
SAMPLING DYNAMICS									
Conversion Time	t_{CONV}	24kHz < f_{CLK} ≤ 2.4MHz	6.667		666.7				µs
Acquisition Time	t_{AQ}	f_{CLK} = 2.4MHz	1.875						µs
Throughout Rate					100				kSPS
Clock Frequency			0.024		2.4				MHz
AC ACCURACY									
Total Harmonic Distortion	THD	2.5Vp-p Sinewave, at 1kHz		–94			*		dB
Spurious-Free Dynamic Range	SFDR	2.5Vp-p Sinewave, at 1kHz		–96			*		dB
Signal-to-Noise Ratio	SNR			–85			–86		dB
Signal-to-Noise + Distortion	SINAD	2.5Vp-p Sinewave, at 1kHz		–85			–85.5		dB
Effective Number of Bits	ENOB			13.8			13.9		Bits
VOLTAGE REFERENCE INPUT									
Reference Voltage			2.5		V_{DD} + 0.3	*		*	V
Reference Input Resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			*		kΩ
		$\overline{CS}$ = V_{DD}		5			*		GΩ
Reference Input Capacitance				20			*		pF
Reference Input Current				0.5	0.75		*	*	mA
		$\overline{CS}$ = V_{DD}		0.1			*		µA
DIGITAL INPUTS(1)									
Logic Family				LVCMOS			*		
High-Level Input Voltage	V_{IH}	V_{DD} = 3.6V	2		V_{DD} + 0.3	*		*	V
Low-Level Input Voltage	V_{IL}	V_{DD} = 2.7V	–0.3		0.8	*		*	V
Input Current	I_{IN}	V_I = V_{DD} or GND			±50	*		*	nA
Input Capacitance	C_I			5			*		pF
DIGITAL OUTPUTS(1)									
Logic Family				LVCMOS			*		
High-Level Output Voltage	V_{OH}	V_{DD} = 2.7V, I_{OH} = –100µA	V_{DD} – 0.2			*			V
Low-Level Output Voltage	V_{OL}	V_{DD} = 2.7V, I_{OL} = 100µA			0.2			*	V
High-Impedance-State Output Current	I_{OZ}	$\overline{CS}$ = V_{DD}, V_I = V_{DD} or GND			±50	*		*	nA
Output Capacitance	C_O			5			*		pF
Load Capacitance	C_L				30			*	pF
Data Format				Straight Binary			*		

* indicates the same specifications as the ADS8325I.

NOTE: (1) Applies for 3.0V nominal supply: V_{DD} (min) = 2.7V and V_{DD} (max) = 3.6V.

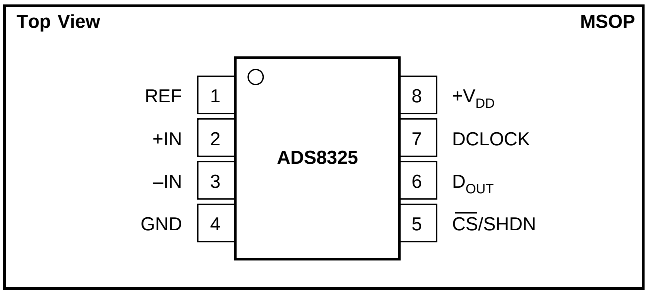
ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature at –40°C to 85°C, $V_{REF} = V_{DD}$, –IN = GND, f_{SAMPLE} = 100kHz, and $f_{CLK} = 24 \bullet f_{SAMPLE}$, unless otherwise noted.

		ADS8325I			ADS8325IB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS								
Power Supply (V_{DD})	Low-Voltage Levels	2.7		3.6	*		*	V
	5V Logic Levels	4.5		5.5	*		*	V
Operating Supply Current (I_{DD})	V_{DD} = 3V		0.75	1.5		*	*	mA
	V_{DD} = 5V		0.9	1.5		*	*	mA
Power-Down Supply Current (I_{DD})	V_{DD} = 3V		0.1			*		µA
	V_{DD} = 5V		0.2			*		µA
Power Dissipation	V_{DD} = 3V		2.25	4.5		*	*	mW
	V_{DD} = 5V		4.5	7.5		*	*	mW
Power Dissipation in Power-Down	V_{DD} = 3V, CS = V_{DD}		0.3			*		µW
	V_{DD} = 5V, CS = V_{DD}		0.6			*		µW

* indicates the same specifications as the ADS8325I.

PIN CONFIGURATION



PIN DESCRIPTIONS

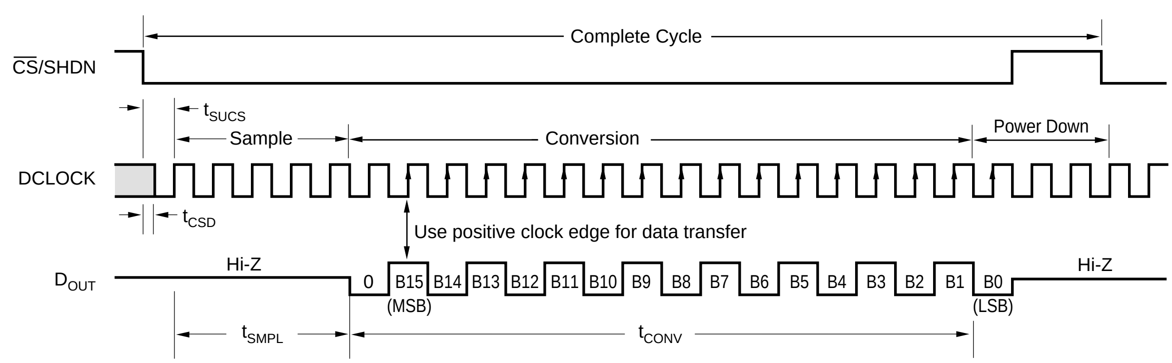
NAME	PIN	I/O	DESCRIPTION
REF	1	AI	Reference Input
+IN	2	AI	Noninverting Input
–IN	3	AI	Inverting Analog Input
GND	4	P	Ground
CS/SHDN	5	DI	Chip Select when LOW, Shutdown Mode when HIGH.
D_{OUT}	6	DO	The serial output data word.
DCLOCK	7	DI	Data Clock synchronizes the serial data transfer and determines conversion speed.
V_{DD}	8	P	Power Supply

NOTE: AI is Analog Input, DI is Digital Input, DO is Digital Output, and P is Power-Supply Connection.

TIMING CHARACTERISTICS

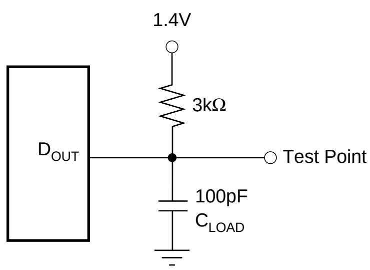
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	4.5		5.0	Clk Cycles
t_{CONV}	Conversion Time		16		Clk Cycles
t_{CYC}	Throughput Rate			100	kHz
t_{CSD}	CS Falling to DCLOCK LOW			0	ns
t_{SUCS}	CS Falling to DCLOCK Rising	20			ns
t_{HDO}	DCLOCK Falling to Current D_{OUT} Not Valid	5	15		ns
t_{DIS}	CS Rising to D_{OUT} Tri-State		70	100	ns
t_{EN}	DCLOCK Falling to D_{OUT} Enabled		20	50	ns
t_F	D_{OUT} Fall Time		5	25	ns
t_R	D_{OUT} Rise Time		7	25	ns

TIMING DIAGRAMS



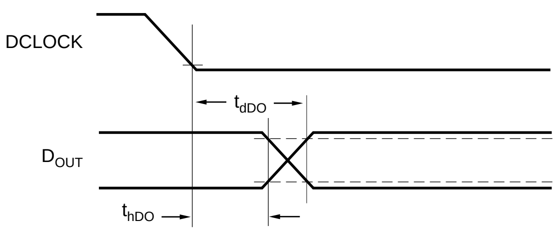
NOTE: A minimum of 22 clock cycles are required for 16-bit conversion. Shown are 24 clock cycles.
If CS remains LOW at the end of conversion, a new datastream with LSB-first is shifted out again.

Timing Diagrams and Test Circuits for the Parameters in the Timing Characteristics table.

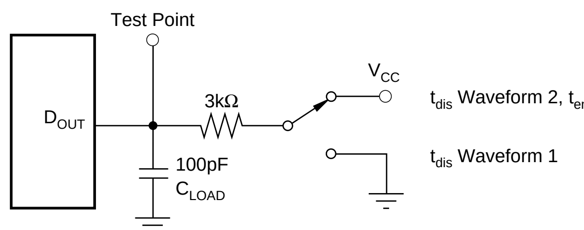


Load Circuit for t_{dDO}, t_r, and t_f

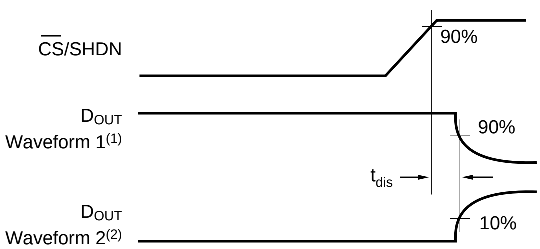
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



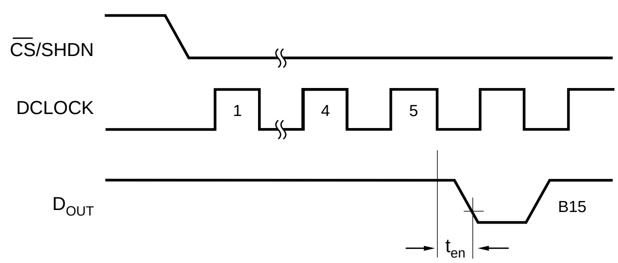
Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}

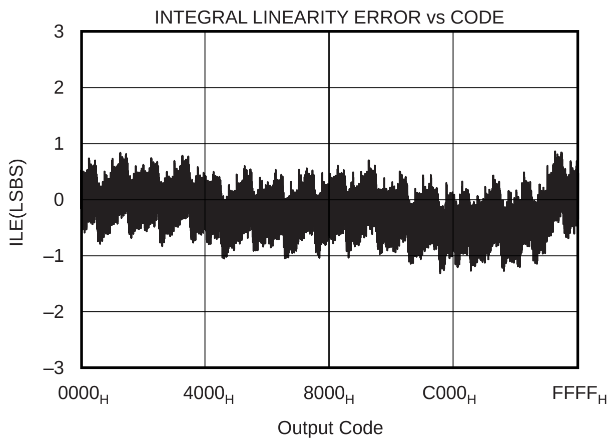


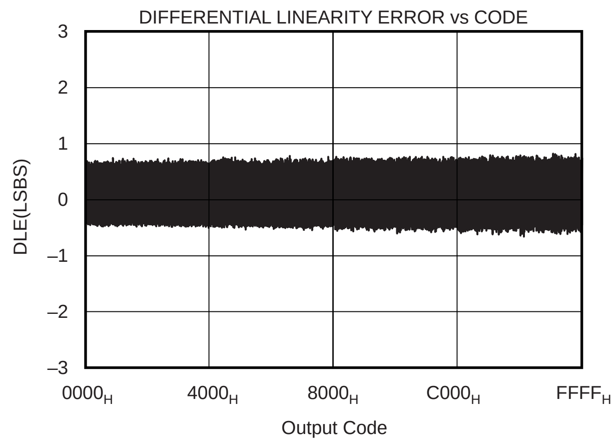
Voltage Waveforms for t_{en}

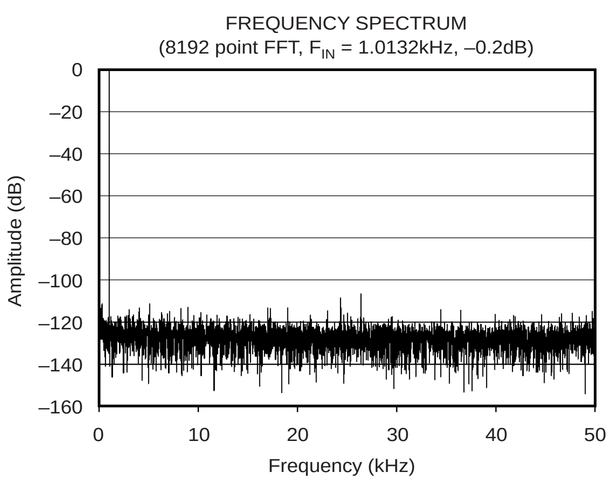
NOTES: (1) Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control. (2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

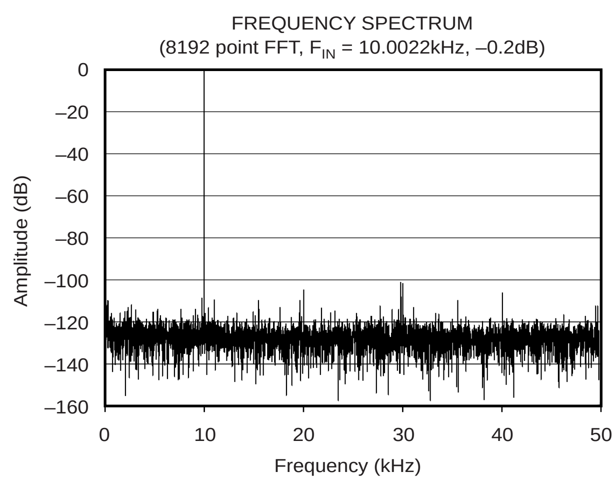
TYPICAL CHARACTERISTICS: V_{DD} = +5V

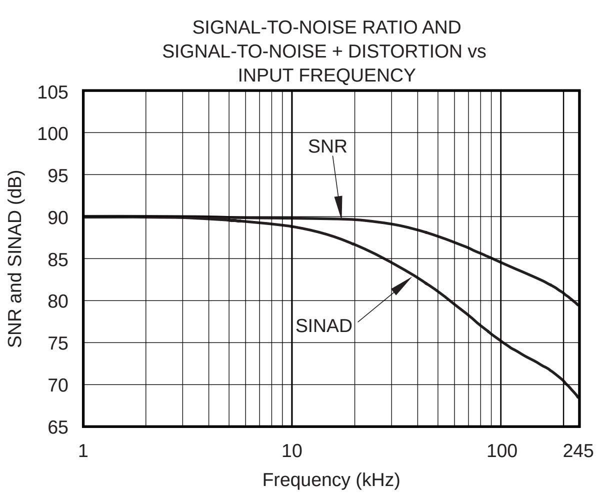
At T_A = 25°C, V_{DD} = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 • f_{SAMPLE}, unless otherwise noted.

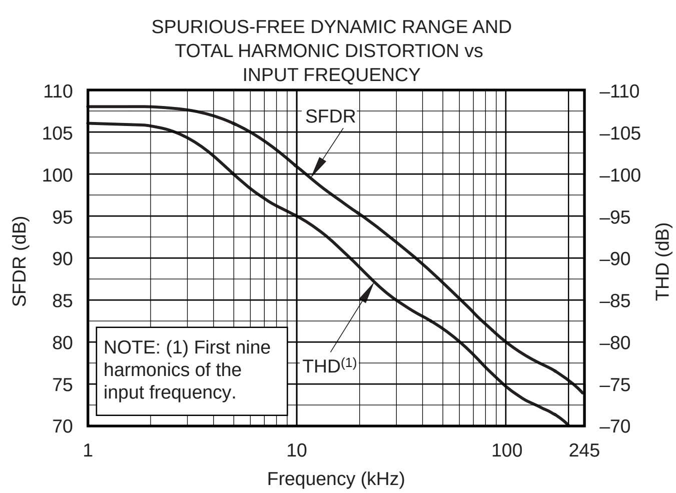






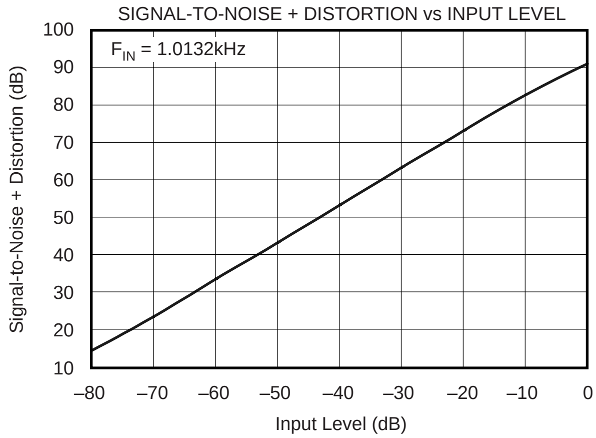


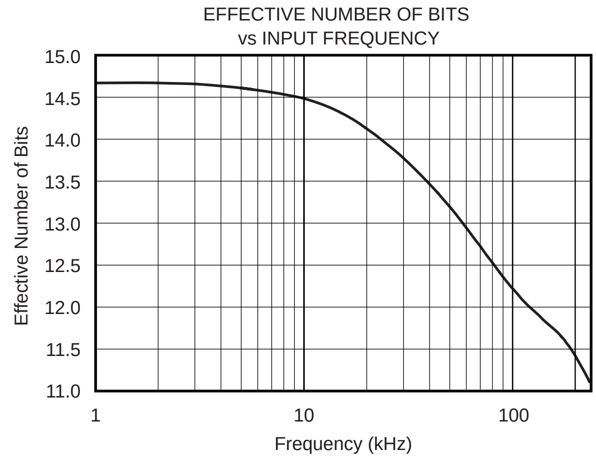


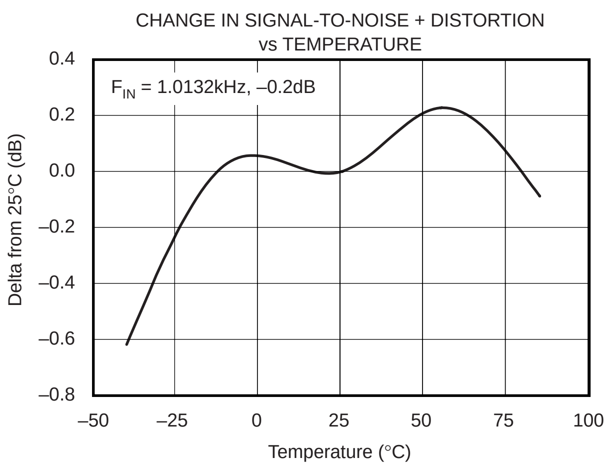


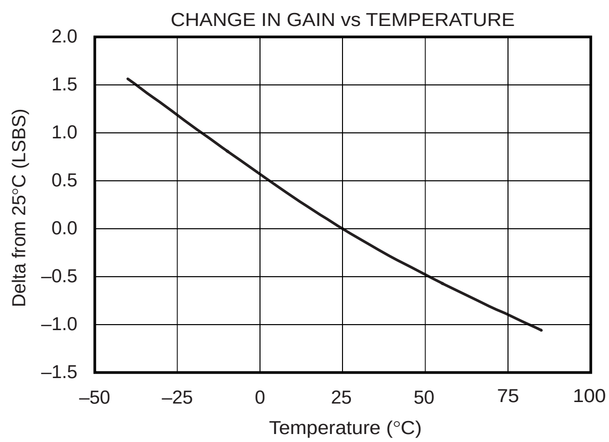
TYPICAL CHARACTERISTICS: V_{DD} = +5V (Cont.)

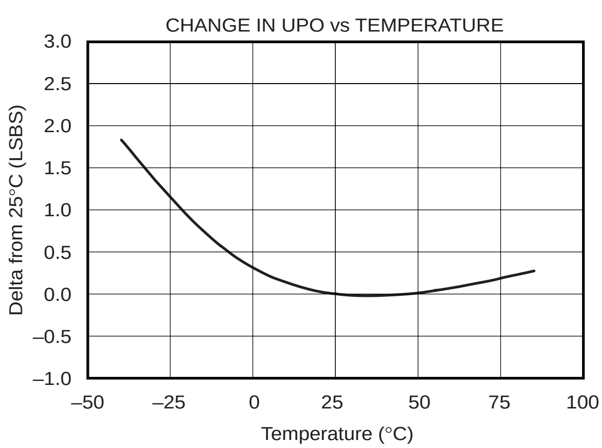
At T_A = 25°C, V_{DD} = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 • f_{SAMPLE}, unless otherwise noted.

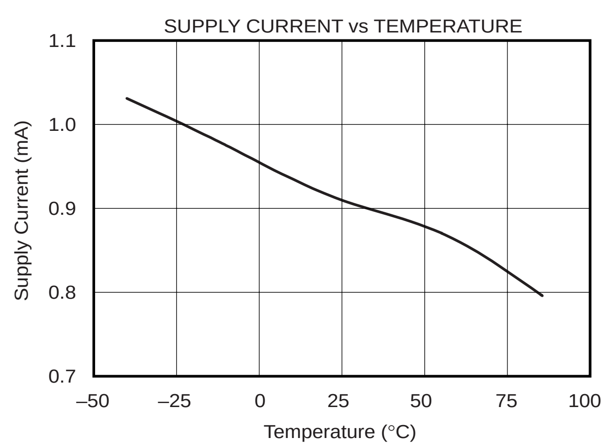






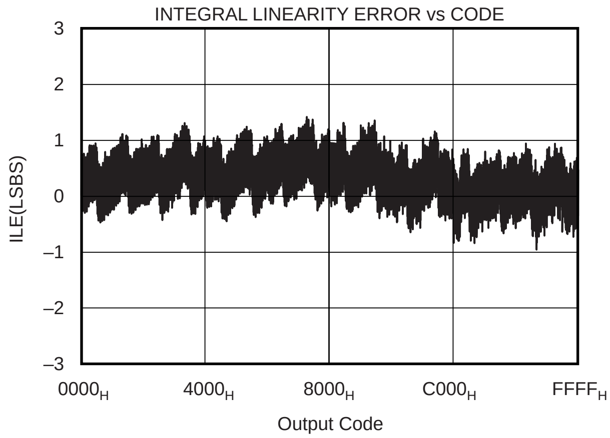


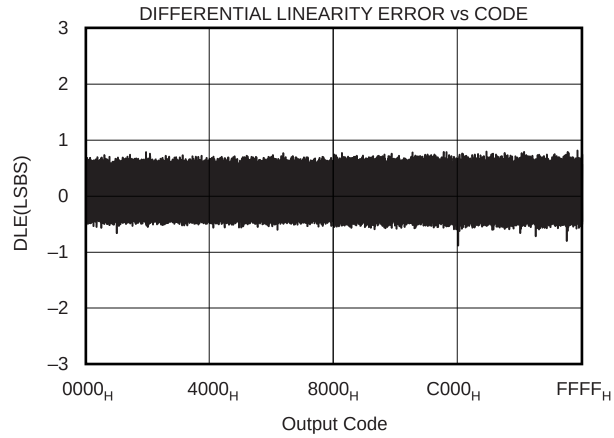


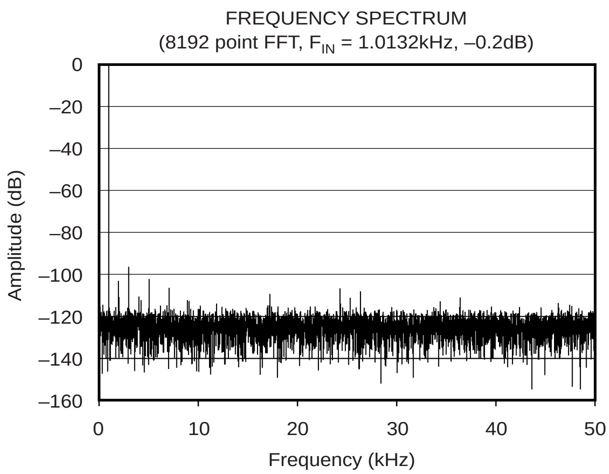


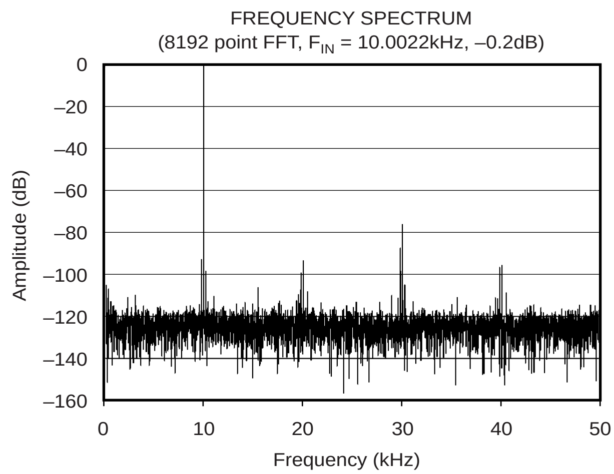
TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

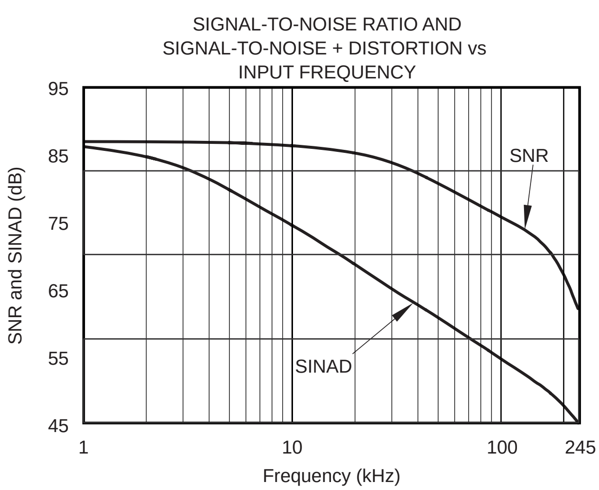
At T_A = 25°C, V_{DD} = 2.7V, V_{REF} = 2.5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 • f_{SAMPLE}, unless otherwise noted.

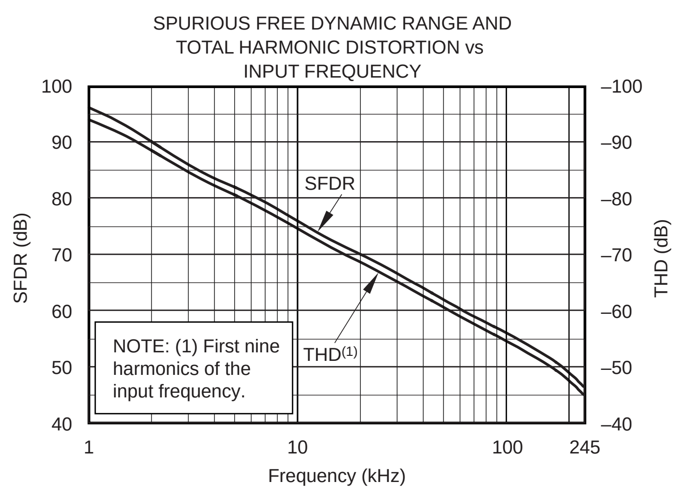






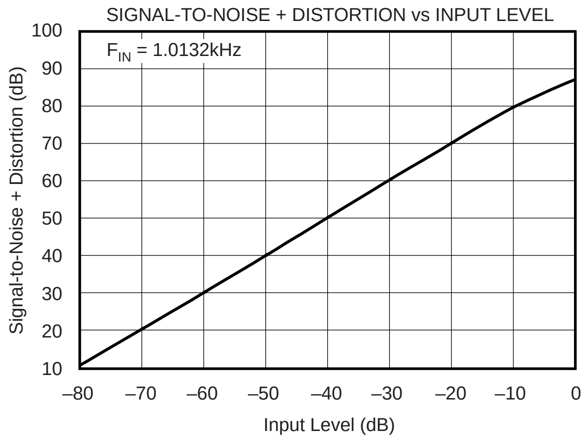


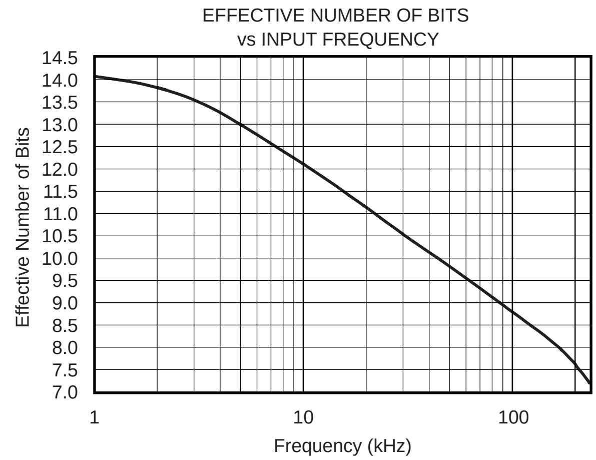


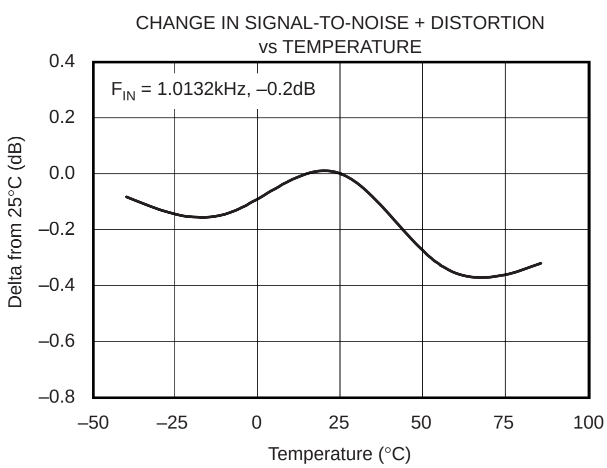


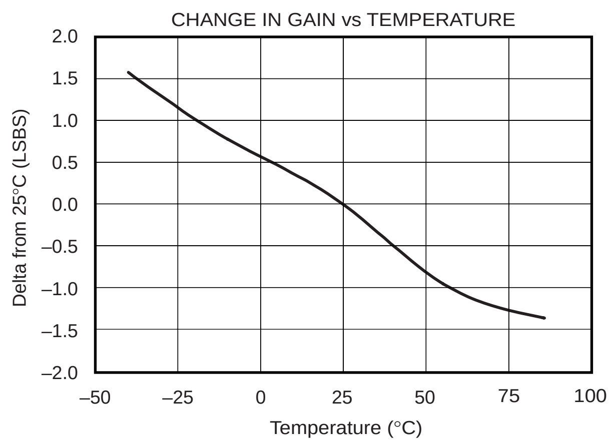
TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (Cont.)

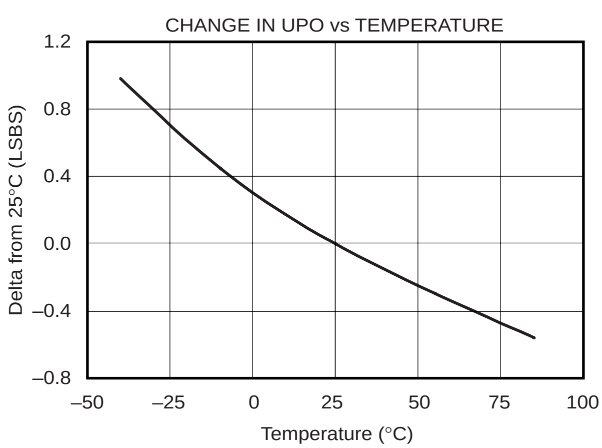
At T_A = 25°C, V_{DD} = 2.7V, V_{REF} = 2.5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 • f_{SAMPLE}, unless otherwise noted.

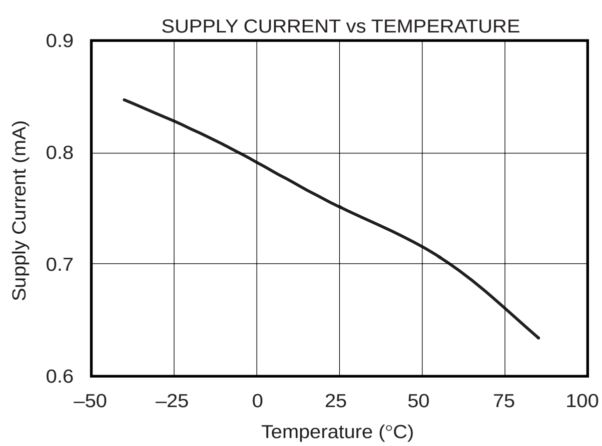












THEORY OF OPERATION

The ADS8325 is a classic Successive Approximation Register (SAR) Analog-to-Digital (A/D) converter. The architecture is based on capacitive redistribution that inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS8325 to acquire and convert an analog signal at up to 100,000 conversions per second while consuming less than 4.5mW from $+V_{DD}$.

The ADS8325 requires an external reference, an external clock, and a single power source (V_{DD}). The external reference can be any voltage between 2.5V and 5.5V. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8325.

The external clock can vary between 24kHz (1kHz throughput) and 2.4MHz (100kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 200ns (V_{DD} = 4.75V or greater). The minimum clock frequency is set by the leakage on the internal capacitors to the ADS8325.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8325 after the conversion is complete and to obtain the serial data least significant bit first. See the Digital Timing section for more information.

ANALOG INPUT

The analog input of ADS8325 is differential. The +IN and –IN input pins allow for a differential input signal. The amplitude of the input is the difference between the +IN and –IN input, or (+IN) – (–IN). Unlike some converters of this type, the –IN input is not resampled later in the conversion cycle. When the converter goes into the hold mode or conversion, the voltage difference between +IN and –IN is captured on the internal capacitor array.

The range of the –IN input is limited to –0.3V to +0.5V. Due to this, the differential input could be used to reject signals that are common to both inputs in the specified range. Thus, the –IN input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The general method for driving the analog input of the ADS8325 is shown in Figures 1 and 2. The –IN input is held at the common-mode voltage. The +IN input swings from –IN (or common-mode voltage) to –IN + V_{REF} (or common-mode voltage + V_{REF}), and the peak-to-peak amplitude is $+V_{REF}$. The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 3). Figures 5 and 6 illustrate the typical change in gain and offset as a function of the common-mode voltage applied to the –IN pin.

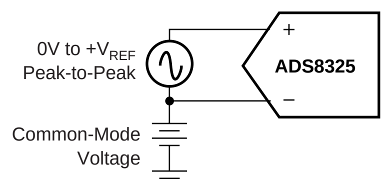
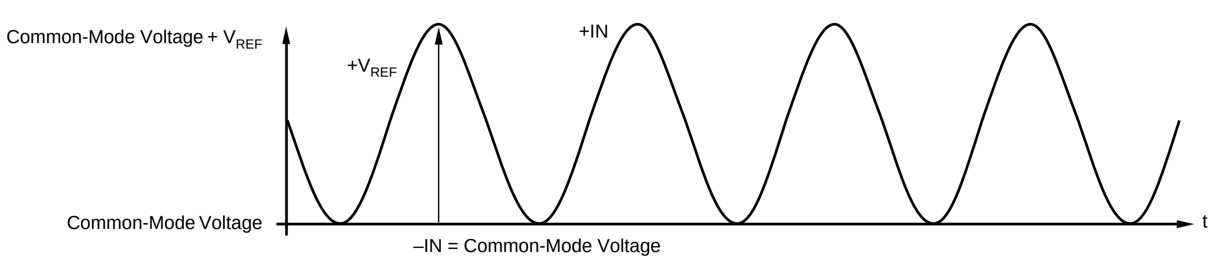


FIGURE 2. Methods of Driving the ADS8325

The input current required by the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS8325 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (20pF) to a 16-bit settling level within 4.5 clock cycles (1.875µs). When the converter goes into the hold mode, or while it is in the power-down mode, the input impedance is greater than 1GΩ.



NOTE: The maximum differential voltage between +IN and –IN of the ADS8325 is V_{REF}.
See Figure 3 for a further explanation of the common-mode voltage range for differential inputs.

FIGURE 1. Differential Input Mode of the ADS8325.

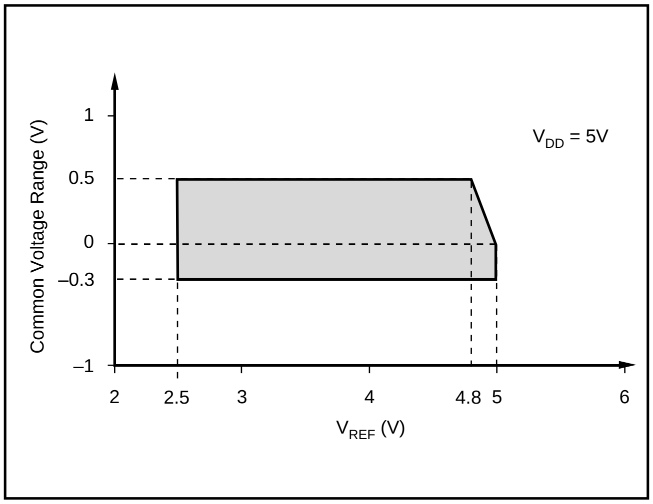


FIGURE 3. +IN Analog Input: Common-Mode Voltage Range vs V_{REF}.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –IN input should not drop below GND – 0.3V or exceed GND + 0.5V. The +IN input should always remain within the range of GND – 0.3V to V_{DD} + 0.3V, or –IN to –IN + V_{REF}, whichever limit is reached first. Outside of these ranges, the converter's linearity may not meet specifications.

To minimize noise, low bandwidth input signals with low-pass filters should be used. In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Often, a small capacitor (20pF) between the positive and negative inputs helps to match their impedance. To obtain maximum performance from the ADS8325, the input circuit from Figure 4 is recommended.

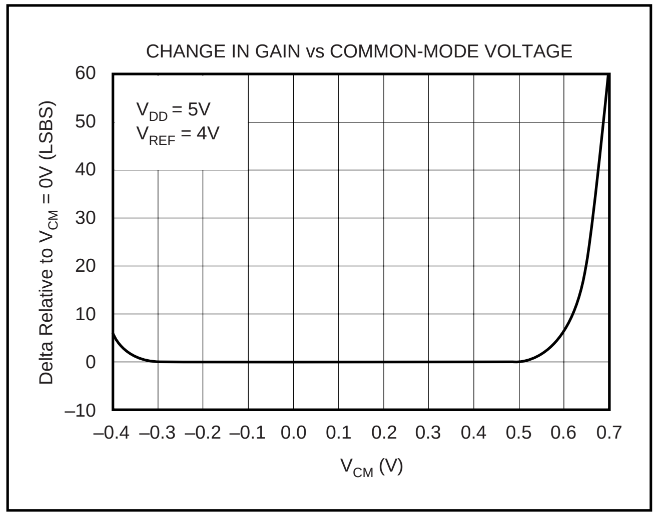


FIGURE 5. Change in Gain vs Common-Mode Voltage.

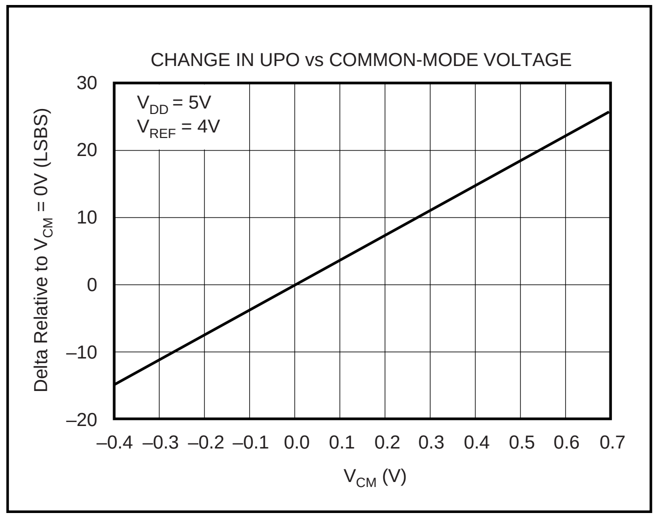


FIGURE 6. Change in Unipolar Offset vs Common-Mode Voltage.

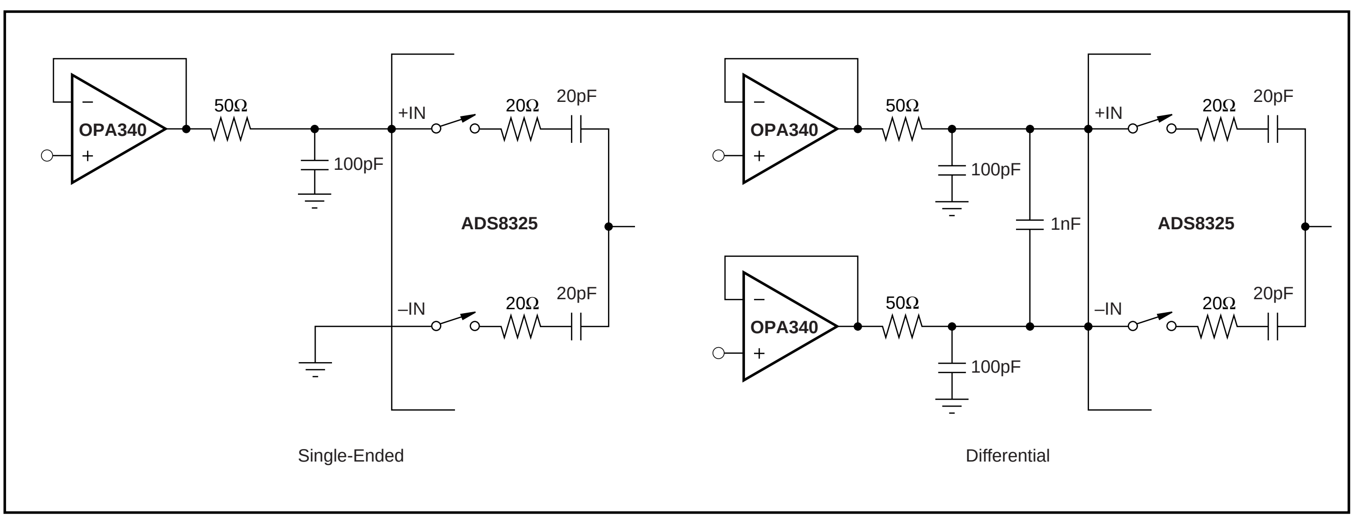


FIGURE 4. Single-Ended and Differential Methods of Interfacing the ADS8325.

REFERENCE INPUT

The external reference sets the analog input range. The ADS8325 will operate with a reference in the range of 2.5V to V_{DD}. There are several important implications to this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to the reference voltage divided by 65,536. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For a reference voltage of 2.5V, the value of LSB is 38.15µV, and for reference voltage of 5V, the LSB is 76.3µV.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 5V reference, the internal noise of the converter typically contributes only 1.5LSBs peak-to-peak of potential error to the output code. When the external reference is 2.5V, the potential error contribution from the internal noise will be 2 times larger (3LSBs). The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical characteristic "Peak-to-Peak Noise vs Reference Voltage." Note that the Effective Number Of Bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows:

$$SINAD = 6.02 \cdot ENOB + 1.76$$

As the difference between the power-supply voltage and reference voltage increases, the gain and offset performance of the converter will decrease. Figure 7 shows the typical change in gain and offset as a function of the difference between the power-supply voltage and reference voltage. For the combination of V_{DD} = 2.7V and V_{REF} = 2.5V, or V_{DD} = 5V and V_{REF} = 5V, offset and gain error will be minimal. The most dramatic difference in offset can be seen when V_{DD} = 5V and V_{REF} = 2.5V.

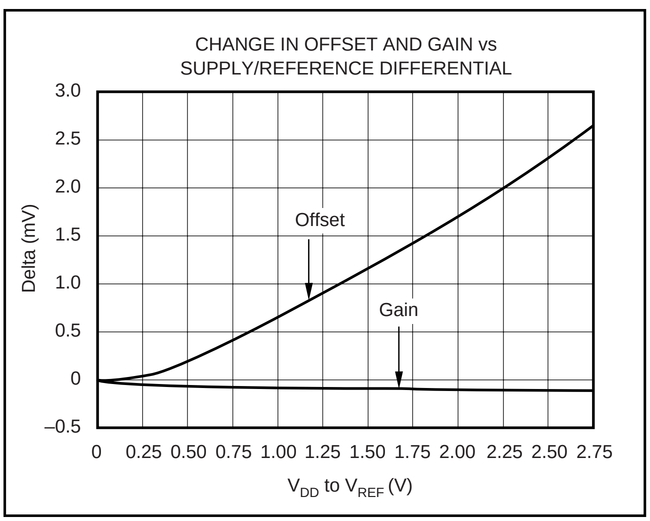


FIGURE 7. Change in Offset and Gain versus the Difference between Power-Supply and Reference Voltage.

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Due to the lower LSB size, the converter will also be more sensitive to external sources of error, such as nearby digital signals and electromagnetic interference.

The equivalent input circuit for the reference voltage is presented in the Figure 8. The 5kΩ resistor presents a constant load during the conversion process. At the same time, an equivalent capacitor of 20pF is switched. To obtain optimum performance from the ADS8325, special care must be taken in designing the interface circuit to the reference input pin. To ensure a stable reference voltage, a 47µF tantalum capacitor with low ESR should be connected as close as possible to the input pin. If a high output impedance reference source is used, an additional operational amplifier with a current limiting resistor must be placed in front of the capacitors.

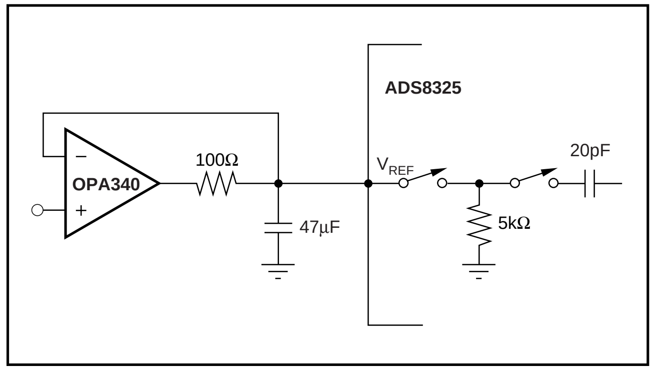


FIGURE 8. Input Reference Circuit and its Interface.

When the ADS8325 is in power-down mode, the input resistance of the reference pin will have a value of 5GΩ. Since the input capacitors must be recharged before the next conversion starts, an operational amplifier with good dynamic characteristics must be used to buffer the reference input.

NOISE

The transition noise of the ADS8325 itself is extremely low (see Figures 9 and 10); it is much lower than competing A/D converters. These histograms were generated by applying a low-noise DC input and initiating 5000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8325. This is true for all 16-bit, SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. The ADS8325, with < 3 output codes for the ±3σ distribution, will yield a < ±0.5LSBs of transition noise. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

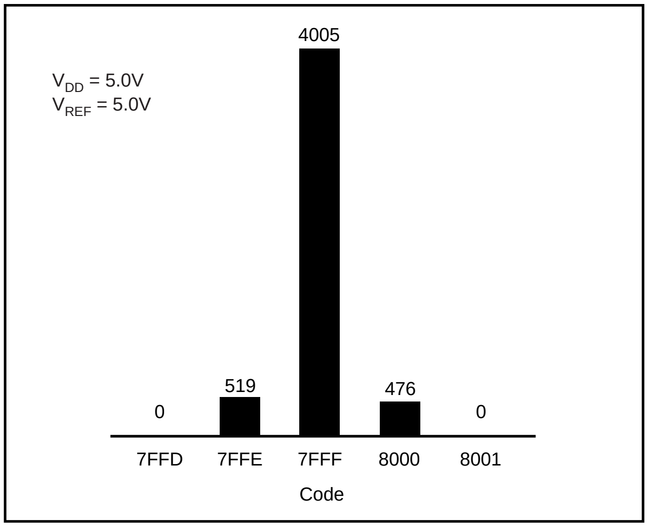


FIGURE 9. 5000 Conversion Histogram of a DC Input.

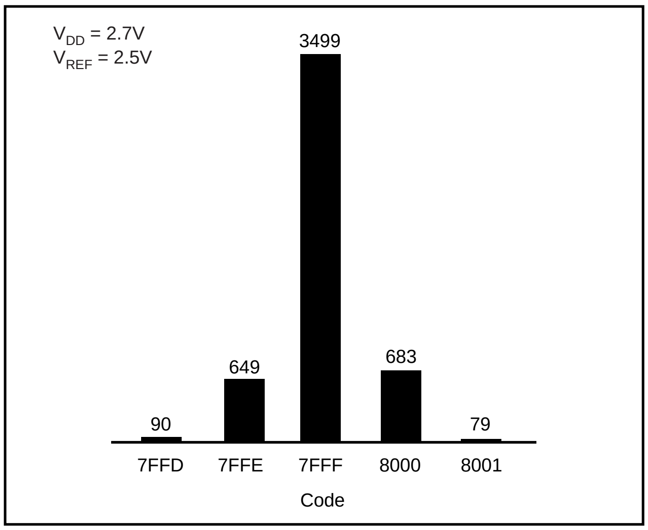


FIGURE 10. 5000 Conversion Histogram of a DC Input.

AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging four conversion results will reduce the transition noise from ±0.5LSB to ±0.25LSB. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio will improve 3dB.

DIGITAL INTERFACE

SIGNAL LEVELS

The ADS8325 has a wide range of power-supply voltage. The A/D converter, as well as the digital interface circuit, is designed to accept and operate from 2.7V up to 5.5V. This voltage range will accommodate different logic levels.

When the ADS8325's power-supply voltage is in the range of 4.5V to 5.5V (5V logic level), the ADS8325 can be connected directly to another 5V CMOS integrated circuit.

Another possibility is that the ADS8325's power-supply voltage is in the range of 2.7V to 3.6V. The ADS8325 can be connected directly to another 3.3V LVCMOS integrated circuit.

SERIAL INTERFACE

The ADS8325 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as illustrated in the Timing Diagram and Timing Characteristics table. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling DCLOCK edge, D_{OUT} is enabled and will output a LOW value for one clock period. For the next 16 DCLOCK periods, D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data, but in a least significant bit first format.

After the most significant bit (B15) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

DATA FORMAT

The output data from the ADS8325 is in Straight Binary format (see Figure 11). This figure represents the ideal output code for a given input voltage and does not include the effects of offset, gain error, or noise.

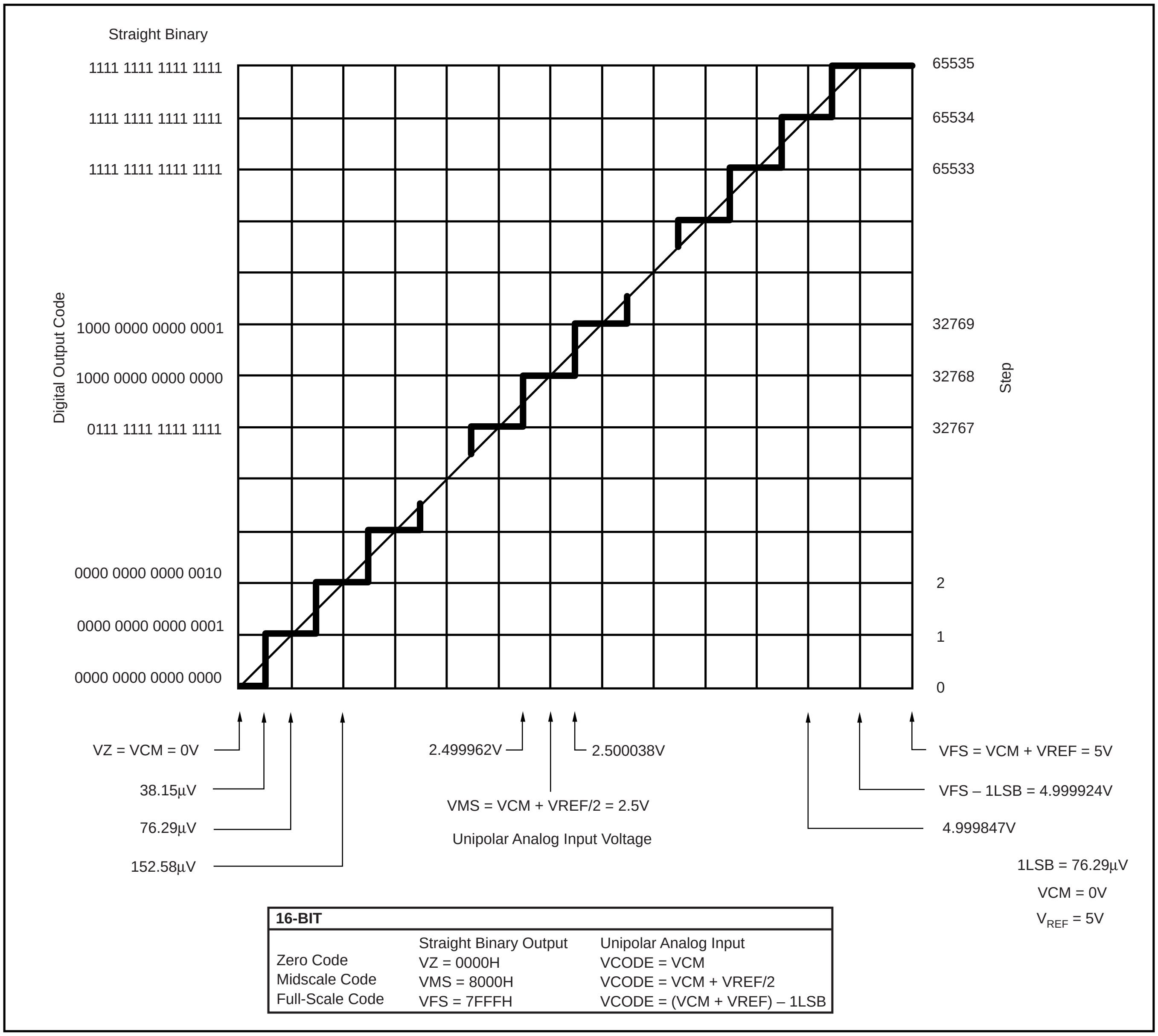


FIGURE 11. Ideal Conversion Characteristics (Condition: VCM = 0V, VREF = 5V).

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design, allow the ADS8325 to convert at up to a 100kHz rate while requiring very little power. However, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS8325 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS8325 is in power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (see Timing Diagram). Ideally, each conversion should occur as quickly as possible, preferably at a 2.4MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously until the power-down mode is entered.

See Figures 12 and 13 for the current consumption of the ADS8325 versus sample rate. For these graphs, the converter is clocked at 2.4MHz regardless of the sample rate. $\overline{CS}$ is held HIGH during the remaining sample period.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode that is enabled when $\overline{CS}$ is HIGH. $\overline{CS}$ LOW will shutdown only the analog section. The digital section is completely shutdown only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion, and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH.

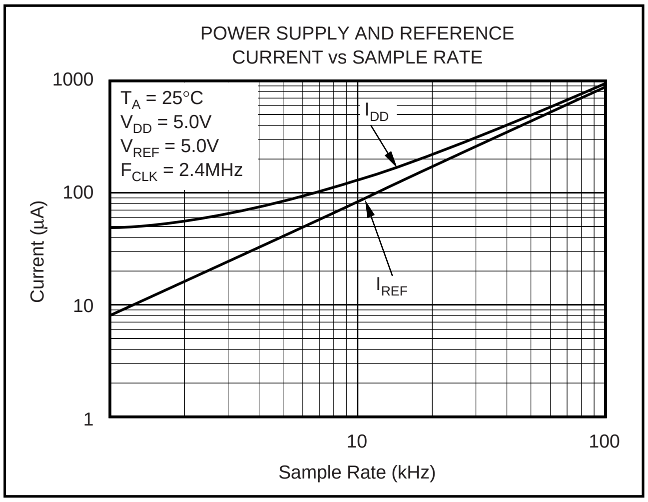


FIGURE 12. Power-Supply and Reference Current vs Sample Rate at V_{DD} = 5V.

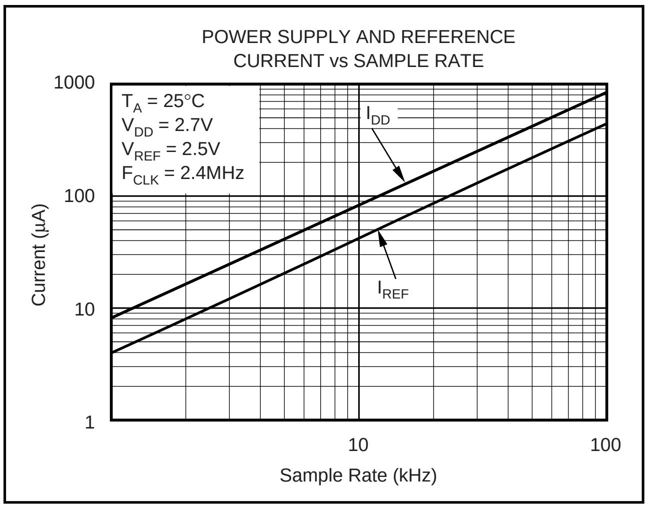


FIGURE 13. Power-Supply and Reference Current vs Sample Rate at V_{DD} = 2.7V.

SHORT CYCLING

Another way to save power is to utilize the $\overline{CS}$ signal to short cycle the conversion. Due to the ADS8325 placing the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 14th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be needed. If so, the conversion can be terminated after the first n bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system as they spend more time in power-down mode.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8325 circuitry. This will be particularly true if the reference voltage is low and/or the conversion rate is high. At a 100kHz conversion rate, the ADS8325 makes a bit decision every 416ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high-power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter's DCLOCK signal as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS8325 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close as possible to the ADS8325 package. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 47µF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS8325 draws very little current from the reference on average, there are still instantaneous current demands placed on the external input and reference circuitry.

Texas Instrument's OPA627 op amp provides optimum performance for buffering both the signal and reference inputs. For low-cost, low-voltage, single-supply applications, the OPA2350 or OPA2340 dual op amps are recommended.

Also, keep in mind that the ADS8325 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin on the ADS8325 should be placed on a clean ground point. In many cases, this will be the "analog" ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figure 14 shows a basic data acquisition system. The ADS8325 input range is connected to 2.5V or 4.096V. The 5Ω resistor and 1µF to 10µF capacitor filters the microcontroller "noise" on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of noise. Operational amplifiers and voltage reference are connected to analog power supply, AV_{DD}.

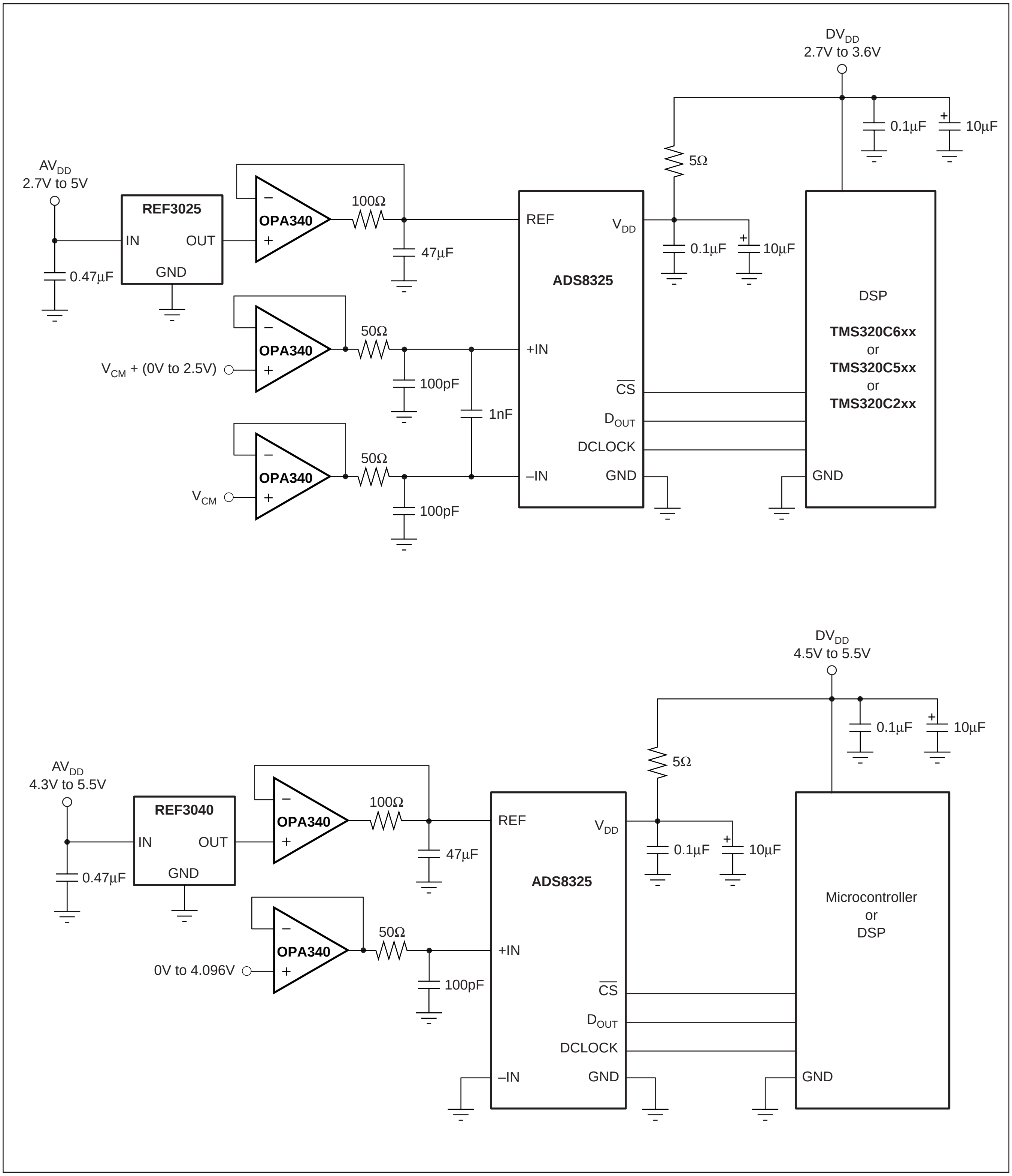
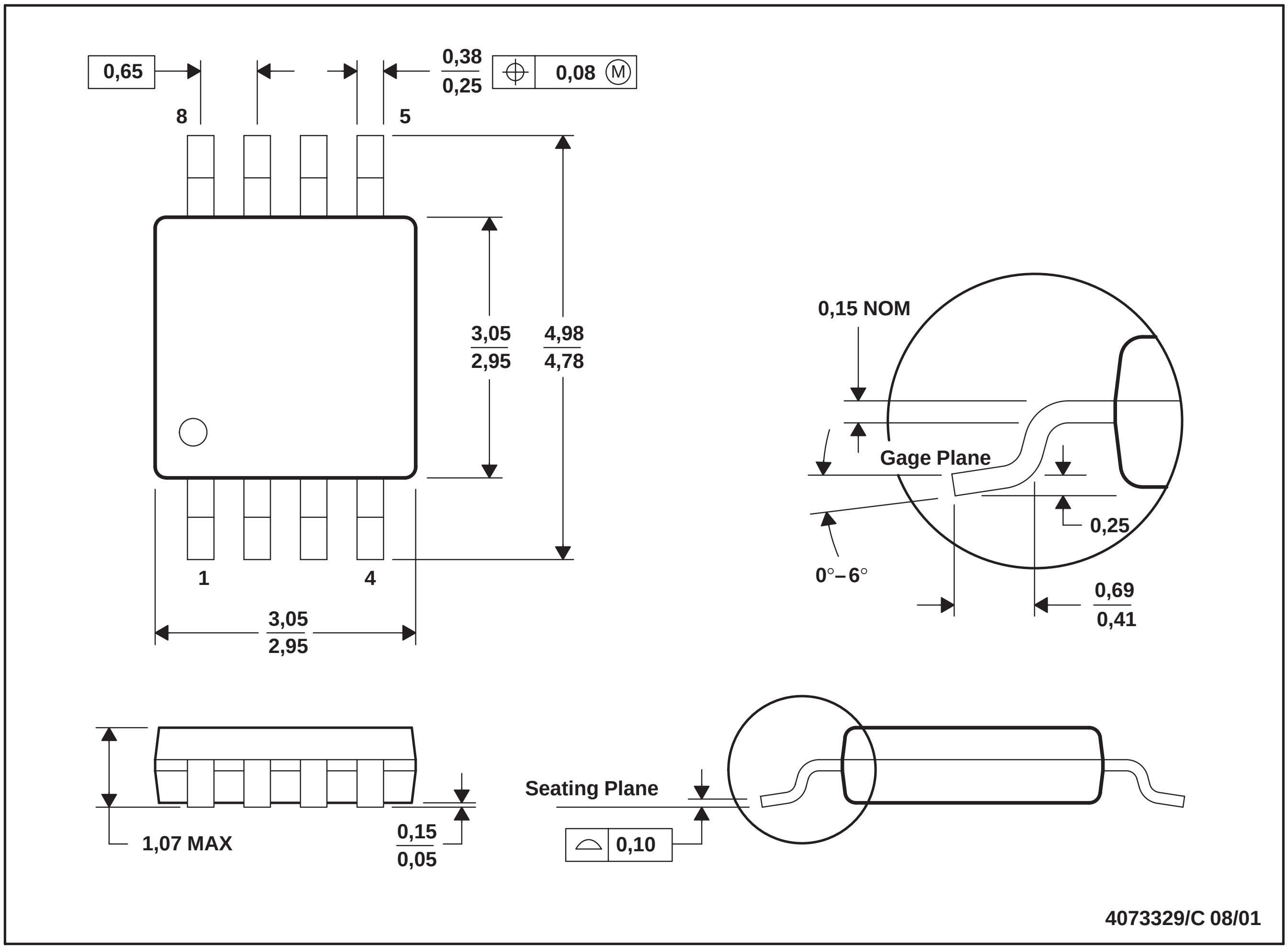


FIGURE 14. Two Examples of a Basic Data Acquisition System.

DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

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